# JOB OPENING

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| **Analog Design Engineer** | Design and optimize Analog IPs including IO library, DLL, PLL, Power Management, data converters. | • **Education:** Bachelor/Master of Electrical Engineering or equivalent.  
  • **Experience:**  
    - IC1: Fresh  
    - IC2: 2-3 years  
    - IC3: 4-5 years.  
  • **Technical:**  
    - Familiar with design tools: SNSP, Cadence schematic/layout entry, HSPICE, Verilog;  
    - CMOS design.  
    - Synopsys tools for schematic/layout entry (or Cadence equivalent tools)  
    - Perl, C-shell scripting. | 6 IC1 – DN  
1 IC2 – DN  
1 IC3 – DN  
1 IC2 - HCM |
| **Circuit Design Engineer** | Design and optimize embedded IPs including memory compilers, IO library and standard cells library using CMOS technology. | • **Education:** Bachelor/Master of Electrical Engineering  
  • **Experience:**  
    - IC1: Fresh  
    - IC2: 2-3 years  
    - IC3: 4-5 years.  
  • **Technical:**  
    - Strong background in Semiconductor Physics and Logical Analytics  
    - Familiar in using circuit and logic simulation tools (Cadence/HSPICE/HSIM...) | 4 IC1 – DN  
4 IC1 - HCM/DN  
4 IC1 - HCM  
1 IC3 - HCM |
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| **Circuit Design Manager**         | Exercises full line management responsibilities including resource development and relatives, manages through subordinate supervisors, and/or directly manages professional (exempt) individual contributors (mix of subordinates varies based on the function) to complete works assigned to the function, including IPs development, IPs design services, as well as design methodology & process development. | • **Education:** Bachelor/Master of Electrical Engineering.  
  • **Experience:** more than 5 years.  
  • **Technical:**  
  - Knowledge of transistor-level CMOS design, analog mixed-signal circuit design and embedded memory design  
  - Knowledge of design methodology, EDA views, Custom IC design EDA tools and QA procedure  
  - Device evaluation and characterization, analog layout, DRC/LVS, RC parasitic extraction, library characterization.  
  - Good knowledge of programming language: PHP, Shell, Perl, Java  
  - Good knowledge of Windows environment: AD, Group policy, SMB, Domain and MS Office | 1 IC4/M3 – HCM.  
  1 IC4/M2 – HCM. |
| **Physical Design Engineer (ASIC)** | The position main responsibility consists of the physical design flow from Netlist to GDSII, physical synthesis, verification and finalization for the design. | • **Education:** Bachelor/Master of Electronics, Telecommunication, Computer Science.  
  • **Experience:** 4-5 years. | 1 IC3 – HCM. |
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| **Physical Design Engineer (IP)**  | Do layout design for Memory IPs, Standard Cells, IOs.                            | • **Education:** Bachelor/Master of Electronics, Telecommunication, Computer Science.  
• **Experience:**  
  - IC1: Fresh  
  - IC2: 2-3 years  
  - IC3: 4-5 years.  
• **Technical:**  
  - Hands on experience with detailed exposure to an actual SoC physical design in STA, Floor-Planning, Power Analysis, CTS, Routing, DRC/LVS and Noise Analysis using Magma or Synopsys ASIC physical design tools.  
  - Scripting language with Perl, Tk/Tcl, AWK, Shell  
  - Synopsys ICC, Talus or other P&R tools | 5 IC1 – DN  
15 IC1 – HCM  
2 IC3 – HCM. |
| **Software Testing Engineer**      | This person will be part of eSilicon’s worldwide Software QA team in testing and certifying production management products. | • **Education:** Bachelor/Master of Computer Science / Math / Information Technology.  
• **Experience:** IC1: Fresh | 1 IC1 - HCM |
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| **Software Developer**  | Develop CAD tools to automate designs, design/QA/QC flows, and data management.                                                                                                                                                                                            | • **Education:** Bachelor/Master of Computer Science / Math / Information Technology / EE.  
• **Experience:**  
  - IC1: Fresh  
  - IC2: 2-3 years  
  - IC3: 4-5 years.  
• **Technical:**  
  - Programming languages (One of): PHP, Shell, Perl, Java, C/C++ TCL, Python, SKILL  
  - Basic knowledge of Linux  
  - Knowledge of EDA tools                                                                 | 1 IC1 – DN  
1 IC1 – HCM  
2 IC3 - HCM |
| **Senior .Net Developer** | Become part of eSilicon team that is building the next generation of eSilicon Access/Virtual Manufacturing system Infrastructure - a critical piece of eSilicon’s business systems. The position offers opportunity to work on patented internal application infrastructure and various supply chain business process automation projects using Microsoft .Net, Microsoft Sharepoint 2010 and Services Oriented platforms. | • **Education:** Bachelor/Master of Computer Science or equivalent  
• **Experience:**  
  - IC1: Fresh  
  - IC2: 2-3 years  
  - IC3: 4-5 years.  
• **Technical:**  
  - Experience working with OOP  
  - Experience working in C#  
  - Good knowledge of .NET 3.5  
  - Two or more years of experience with RDBMS(SQL Server, MYSQL)                                                                 | 1 IC3 – HCM. |
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| Intern    | Will work in IPDE team to support 1 of the below items:  
- Standard Cell Library development  
- Standard Cell Library Development  
- SKILL Library for PCELL development  
- SCU testing  
- Website development | • **Education**: Bachelor/Master of Electrical Engineering or software.  
• **Experience**: Fresh. | 3 in DN |